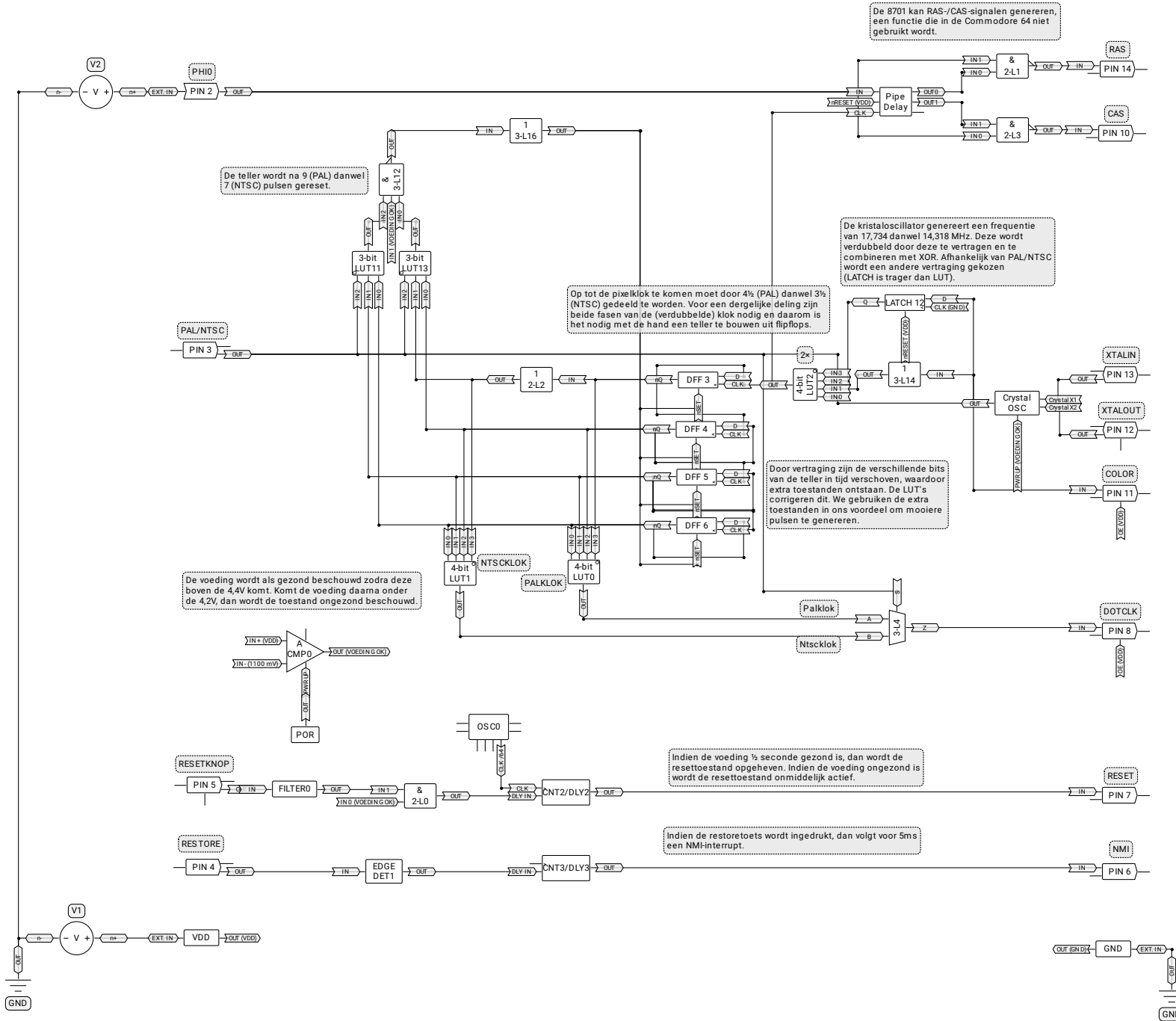


Vervanging van de MOS Technology 8701



VDD (PIN 1)	
<i>Property</i>	<i>Value</i>
Min. value (V)	4.50
Typ. value (V)	5.00
Max. value (V)	5.50

PIN 2 Label: "PHI0"	
<i>Property</i>	<i>Value</i>
I/O selection	Digital input
In mode	Digital in without Schmitt trigger
Out mode	None
Resistor	Pull Down
Resistor value	1M

PIN 3 Label: "PAL/NTSC"	
<i>Property</i>	<i>Value</i>
I/O selection	Digital input
In mode	Digital in without Schmitt trigger
Out mode	None
Resistor	Pull Up
Resistor value	10K

PIN 4 Label: "RESTORE"	
<i>Property</i>	<i>Value</i>
I/O selection	Digital input
In mode	Low voltage digital input
Out mode	None
Resistor	Pull Up
Resistor value	10K

PIN 5 Label: "RESETKNOP"	
<i>Property</i>	<i>Value</i>
I/O selection	Digital input
In mode	Low voltage digital input
Out mode	None
Resistor	Pull Up
Resistor value	10K

PIN 6 Label: "NMI"	
<i>Property</i>	<i>Value</i>
I/O selection	Digital output
In mode	None
Out mode	1x open drain NMOS
Resistor	Floating

PIN 7 Label: "RESET"	
<i>Property</i>	<i>Value</i>
I/O selection	Digital output
In mode	None
Out mode	1x open drain NMOS
Resistor	Floating

PIN 8 Label: "DOTCLK"	
<i>Property</i>	<i>Value</i>
I/O selection	Digital output
In mode	None
Out mode	1x push pull

PIN 10 Label: "CAS"	
<i>Property</i>	<i>Value</i>
I/O selection	Digital output
In mode	None
Out mode	1x push pull

PIN 11 Label: "COLOR"	
<i>Property</i>	<i>Value</i>
I/O selection	Digital output
In mode	None
Out mode	1x push pull

PIN 12 Label: "XTALOUT"	
<i>Property</i>	<i>Value</i>
I/O selection	Crystal OSC X2
In mode	Analog input/output
Out mode	None

PIN 13 Label: "XTALIN"	
<i>Property</i>	<i>Value</i>
I/O selection	Crystal OSC X1
In mode	Analog input/output
Out mode	None

PIN 14 Label: "RAS"	
<i>Property</i>	<i>Value</i>
I/O selection	Digital output
In mode	None
Out mode	1x push pull

4-bit LUT2 Label: "2x"				
<i>IN3</i>	<i>IN2</i>	<i>IN1</i>	<i>IN0</i>	<i>OUT</i>
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0
<i>Property</i>	<i>Value</i>			
Standard gates	Defined by user			

A CMP0	
<i>Property</i>	<i>Value</i>
Hysteresis	50 mV
Low bandwidth	Enable
IN+ gain	x0.25
IN+ source	VDD
IN- source	1100 mV

FILTER0/EDGE DET0	
<i>Property</i>	<i>Value</i>
Type	FILTER
Output polarity	Normal

FILTER1/EDGE DET1	
<i>Property</i>	<i>Value</i>
Type	EDGE DET
Mode	Falling edge detector

2-bit LUT0/DFF/LATCH0		
<i>IN1</i>	<i>IN0</i>	<i>OUT</i>
0	0	0
0	1	0
1	0	0
1	1	1
<i>Property</i>	<i>Value</i>	
Type	LUT	
Standard gates	AND	

2-bit LUT1/DFF/LATCH1		
<i>IN1</i>	<i>IN0</i>	<i>OUT</i>
0	0	1
0	1	1
1	0	1
1	1	0
<i>Property</i>	<i>Value</i>	
Type	LUT	
Standard gates	NAND	

2-bit LUT2/DFF/LATCH2	
<i>IN</i>	<i>OUT</i>
0	0
1	1
<i>Property</i>	<i>Value</i>
Type	LUT
Standard gates	Buffer

2-bit LUT3/PGEN		
<i>IN1</i>	<i>IN0</i>	<i>OUT</i>
0	0	1
0	1	1
1	0	1
1	1	0
<i>Property</i>	<i>Value</i>	
Type	LUT	
Standard gates	NAND	

3-bit LUT0/DFF/LATCH3	
<i>Property</i>	<i>Value</i>
Type	DFF / LATCH
Mode	DFF
2 consecutive DFFs for ASM	Disable
nSET /nRESET option	nSET
Initial polarity	Low
Q output polarity	Inverted (nQ)

3-bit LUT1/DFF/LATCH4	
<i>Property</i>	<i>Value</i>
Type	DFF / LATCH
Mode	DFF
nSET /nRESET option	nSET
Initial polarity	Low
Q output polarity	Inverted (nQ)

3-bit LUT2/DFF/LATCH5	
<i>Property</i>	<i>Value</i>
Type	DFF / LATCH
Mode	DFF
nSET /nRESET option	nSET
Initial polarity	Low
Q output polarity	Inverted (nQ)

3-bit LUT3/DFF/LATCH6	
<i>Property</i>	<i>Value</i>
Type	DFF / LATCH
Mode	DFF
nSET /nRESET option	nSET
Initial polarity	Low
Q output polarity	Inverted (nQ)

3-bit LUT4/DFF/LATCH7			
<i>S</i>	<i>A</i>	<i>B</i>	<i>Z</i>
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

<i>Property</i>	<i>Value</i>
Type	LUT
Standard gates	Multiplexer

3-bit LUT11/DFF/LATCH8			
<i>IN2</i>	<i>IN1</i>	<i>IN0</i>	<i>OUT</i>
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

<i>Property</i>	<i>Value</i>
Type	LUT
Standard gates	Defined by user

3-bit LUT12/DFF/LATCH9			
<i>IN2</i>	<i>IN1</i>	<i>IN0</i>	<i>OUT</i>
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

<i>Property</i>	<i>Value</i>
Type	LUT
Standard gates	NAND

3-bit LUT13/DFF/LATCH10			
IN2	IN1	IN0	OUT
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Property	Value
Type	LUT
Standard gates	Defined by user

3-bit LUT14/DFF/LATCH11	
IN	OUT
0	0
1	1

Property	Value
Type	LUT
Standard gates	Buffer

3-bit LUT15/DFF/LATCH12	
Property	Value
Type	DFF / LATCH
Mode	LATCH
nSET/nRESET option	nRESET
Initial polarity	Low
Q output polarity	Non-inverted (Q)

3-bit LUT16/DFF/LATCH13	
IN	OUT
0	0
1	1

Property	Value
Type	LUT
Standard gates	Buffer

3-bit LUT5/8-bit CNT2/DLY2	
Property	Value
Type	CNT/DLY
Mode	Delay
Counter data	195
Delay time (typical)	501.76 ms
Edge select	Rising
Output polarity	Non-inverted (OUT)
Clock	OSC0 CLK /64
Clock frequency	390.625 Hz

3-bit LUT6/8-bit CNT3/DLY3	
Property	Value
Type	CNT/DLY
Mode	One shot
Counter data	2
Pulse width (typical)	120 us
Edge select	Rising
Output polarity	Non-inverted (OUT)
Clock	OSC0 CLK
Clock frequency	25 kHz

3-bit LUT10/Pipe Delay	
Property	Value
Type	Pipe Delay
OUT0 PD num	3
OUT1 PD num	7
OUT1 output polarity	Non-inverted (OUT1)

4-bit LUT0/WS Ctrl/16-bit CNT0/DLY0/FSM0				
Label: "PALKLOK"				
IN3	IN2	IN1	IN0	OUT
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Property	Value
Type	LUT
Standard gates	Defined by user

4-bit LUT1/16-bit CNT1/DLY1/FSM1				
Label: "NTSCKLOK"				
<i>IN3</i>	<i>IN2</i>	<i>IN1</i>	<i>IN0</i>	<i>OUT</i>
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1
<i>Property</i>	<i>Value</i>			
Type	LUT			
Standard gates	Defined by user			

Crystal OSC	
<i>Property</i>	<i>Value</i>
Enable crystal oscillator	Enable
Power down	PD for crystal OSC

OSCO	
<i>Property</i>	<i>Value</i>
Control pin mode	Power down
OSC power mode	Auto Power On
Clock selector	OSC
Fast start-up	Disable
RC OSC frequency	25 kHz
'CLK' predivider by	1
'OUT0' second divider by	1
'OUT1' second divider by	1

External Components

V1	
<i>Property</i>	<i>Value</i>
Element	Voltage Source
Internal capacitance	100nF
Internal resistance	100hm
Type	DC
DC Voltage	5V

V2	
<i>Property</i>	<i>Value</i>
Element	Voltage Source
Pre-start delay	0s
Repeat state	Cyclic
Pre-start state	Low
Type	Clock generator
Frequency	1MHz
Duty cycle	50%
Umax	3.3V
Umin	0V
Rise time	0.02μs
Fall time	0.01μs

Project Specs			
	<i>Min.</i>	<i>Typ.</i>	<i>Max.</i>
VDD	4.50	5.00	5.50
Temperature (°C):	0.00	25.00	85.00

General Settings	
Force bandgap on	Disable
Bandgap output delay time	Auto-delay
Power Supply Control mode	Regulator auto ON/OFF and Charge Pump always OFF (use for 3.0V < VDD < 5.5V)
GPIO quick charge	Disable
Pattern ID	1
Lock status	Unlocked

I2C Probing

Probe pins			
Pin	Signal name	Register	In use
GND (PIN 9) -> OUT	GND	HEX: 0xF0`b0 DEC: 240`b0	+
PIN 2 -> OUT	NET 27	HEX: 0xF0`b1 DEC: 240`b1	+
PIN 3 -> OUT	NET 15	HEX: 0xF0`b3 DEC: 240`b3	+
PIN 4 -> OUT	NET 31	HEX: 0xF0`b5 DEC: 240`b5	+
PIN 5 -> OUT	NET 1	HEX: 0xF0`b6 DEC: 240`b6	+
PIN 8 -> OUT		HEX: 0xF0`b7 DEC: 240`b7	-
2-bit LUT 0/DFF/ LAT CH0 -> OUT	NET 19	HEX: 0xF1`b0 DEC: 241`b0	+
2-bit LUT 1/DFF/ LAT CH1 -> OUT	NET 23	HEX: 0xF1`b1 DEC: 241`b1	+
2-bit LUT 2/DFF/ LAT CH2 -> OUT	NET 14	HEX: 0xF1`b2 DEC: 241`b2	+
2-bit LUT 3/PGEN -> OUT	NET 24	HEX: 0xF1`b3 DEC: 241`b3	+
3-bit LUT 0/DFF/ LAT CH3 -> nQ	NET 10	HEX: 0xF1`b4 DEC: 241`b4	+
3-bit LUT 1/DFF/ LAT CH4 -> nQ	NET 11	HEX: 0xF1`b5 DEC: 241`b5	+
3-bit LUT 2/DFF/ LAT CH5 -> nQ	NET 12	HEX: 0xF1`b6 DEC: 241`b6	+
3-bit LUT 3/DFF/ LAT CH6 -> nQ	NET 13	HEX: 0xF1`b7 DEC: 241`b7	+
3-bit LUT 4/DFF/ LAT CH7 -> Z	NET 18	HEX: 0xF2`b0 DEC: 242`b0	+
3-bit LUT 5/8-bit	NET 0	HEX: 0xF2`b1	+

Probe pins			
CNT 2/DLY2 -> OUT		DEC: 242`b1	
3-bit LUT 6/8-bit CNT 3/DLY3 -> OUT	NET 32	HEX: 0xF2`b2 DEC: 242`b2	+
3-bit LUT 7/8-bit CNT 4/DLY4 -> OUT		HEX: 0xF2`b3 DEC: 242`b3	-
3-bit LUT 8/8-bit CNT 5/DLY5 -> OUT		HEX: 0xF2`b4 DEC: 242`b4	-
3-bit LUT 9/8-bit CNT 6/DLY6 -> OUT		HEX: 0xF2`b5 DEC: 242`b5	-
4-bit LUT 0/WS Ctrl/ 16-bit CNT 0/DLY0/ FSM0 -> OUT	NET 16	HEX: 0xF2`b6 DEC: 242`b6	+
4-bit LUT 1/16-bit CNT 1/DLY1/FSM1 - > OUT	NET 17	HEX: 0xF2`b7 DEC: 242`b7	+
3-bit LUT 10/Pipe Delay -> 1 PIPE OUT		HEX: 0xF3`b0 DEC: 243`b0	-
3-bit LUT 10/Pipe Delay -> OUT 0	NET 25	HEX: 0xF3`b1 DEC: 243`b1	+
3-bit LUT 10/Pipe Delay -> OUT 1	NET 26	HEX: 0xF3`b2 DEC: 243`b2	+
OSC0 -> OUT 0		HEX: 0xF3`b3 DEC: 243`b3	-
OSC0 -> OUT 1		HEX: 0xF3`b4 DEC: 243`b4	-
OSC1 -> OUT		HEX: 0xF3`b5 DEC: 243`b5	-
FILT ER0/EDGE DET 0 -> OUT	NET 34	HEX: 0xF3`b6 DEC: 243`b6	+
FILT ER1/EDGE DET 1 -> OUT	NET 33	HEX: 0xF3`b7 DEC: 243`b7	+
PIN 6 -> OUT /I2C ->		HEX: 0xF4`b0	-

Probe pins			
OUT 0		DEC: 244`b0	
PIN 7 -> OUT /I2C -> OUT 1		HEX: 0xF4`b1 DEC: 244`b1	-
I2C -> OUT 2		HEX: 0xF4`b2 DEC: 244`b2	-
I2C -> OUT 3		HEX: 0xF4`b3 DEC: 244`b3	-
I2C -> OUT 4		HEX: 0xF4`b4 DEC: 244`b4	-
I2C -> OUT 5		HEX: 0xF4`b5 DEC: 244`b5	-
I2C -> OUT 6		HEX: 0xF4`b6 DEC: 244`b6	-
I2C -> OUT 7		HEX: 0xF4`b7 DEC: 244`b7	-
3-bit LUT 11/DFF/ LAT CH8 -> OUT	NET 21	HEX: 0xF5`b0 DEC: 245`b0	+
3-bit LUT 12/DFF/ LAT CH9 -> OUT	NET 35	HEX: 0xF5`b1 DEC: 245`b1	+
3-bit LUT 13/DFF/ LAT CH10 -> OUT	NET 20	HEX: 0xF5`b2 DEC: 245`b2	+
3-bit LUT 14/DFF/ LAT CH11 -> OUT	NET 29	HEX: 0xF5`b3 DEC: 245`b3	+
3-bit LUT 15/DFF/ LAT CH12 -> Q	NET 9	HEX: 0xF5`b4 DEC: 245`b4	+
3-bit LUT 16/DFF/ LAT CH13 -> OUT	NET 22	HEX: 0xF5`b5 DEC: 245`b5	+
3-bit LUT 17/DFF/ LAT CH14 -> OUT		HEX: 0xF5`b6 DEC: 245`b6	-
4-bit LUT 2 -> OUT	NET 8	HEX: 0xF5`b7 DEC: 245`b7	+
PIN 10 -> OUT		HEX: 0xF6`b0	-

Probe pins			
		DEC: 246`b0	
PIN 11 -> OUT		HEX: 0xF6`b2 DEC: 246`b2	-
PIN 12 -> OUT	NET 6	HEX: 0xF6`b4 DEC: 246`b4	-
PIN 13 -> OUT / Crystal OSC -> OUT	NET 5/NET 7	HEX: 0xF6`b5 DEC: 246`b5	+
PIN 14 -> OUT		HEX: 0xF7`b0 DEC: 247`b0	-
A CMP0 -> OUT	VOEDING OK	HEX: 0xF7`b1 DEC: 247`b1	+
A CMP1 -> OUT		HEX: 0xF7`b2 DEC: 247`b2	-
A CMP2 -> OUT		HEX: 0xF7`b3 DEC: 247`b3	-
P DLY -> OUT		HEX: 0xF7`b5 DEC: 247`b5	-
POR -> OUT	POR	HEX: 0xF7`b6 DEC: 247`b6	+
VDD (PIN 1) -> OUT	VDD	HEX: 0xF7`b7 DEC: 247`b7	+

Macrocells		
CNT 1/DLY1/FSM1		DEC: 238, 239

Macrocells		
Macrocell	Property	Register
3-bit LUT 7/8-bit CNT 4/DLY4	Counted Data	HEX: 0xEA DEC: 234
3-bit LUT 9/8-bit CNT 6/DLY6	Counted Data	HEX: 0xED DEC: 237
4-bit LUT 0/WS Ctrl/ 16-bit CNT 0/DLY0/ FSM0	Counted Data	HEX: 0xEB, 0xEC DEC: 235, 236
4-bit LUT 1/16-bit	Counted Data	HEX: 0xEE, 0xEF